TRANSMITTAL LETTER (General - Patent Pending)	Docket No. 51889/2

In Re Application Of: **D uglas R. Hackler, Sr. et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
10/613,169	**July 3, 2003**	**Not yet ssigned**	**2811**

Title: **MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Inf rmation Disclosure Statement
PTO-1449 with copies of cited references
Postcard

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☐ The Director is hereby authorized to charge and credit Deposit Account No. as described below.
  - ☐ Charge the amount of
  - ☐ Credit any overpayment.
  - ☐ Charge any additional fee required.

Signature

Dated: **October 31, 2003**

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I certify that this document and fee is being deposited on **Oct. 31, 2003** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

John R. Thompson

Typed or Printed Name of Person Mailing Correspondence

cc:

PATENT APPLICATION
Docket No.: 51889/2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:		
	Douglas R. Hackler, Sr. et al.	Art Unit
Serial No.:	10/613,169	2811
Filed:	July 3, 2003	
For:	MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET	

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R § 1.97

TO THE COMMISSIONER FOR PATENTS:

Pursuant to his (her) (their) duty of disclosure, applicant(s) enclose(s) copies (a copy) of the document(s) listed on the accompanying Form PTO-1449.

1. This information disclosure statement is being submitted:

a. ☒ Within three months of the filing date of the above-identified application or within three months of the date of entry of the national stage, or before the mailing date of the first Office action on the merits, whichever event occurs last. (No statement under 37 CFR 1.97(e) is required.)

b. ☐ After the period set forth in paragraph 1a, but before the mailing date of either a final action or a notice of allowance. (Check box i. or ii.)

i. ☐ A $180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed.

ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below.

c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of an issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. A petition requesting consideration of the information disclosure statement and the $130.00 petition fee set forth in 37 CFR 1.17(i) are enclosed.

d. ☐ Concurrent with the filing of a Request for Continued Examination

2. ☐ The attorney or agent signing below hereby states that:

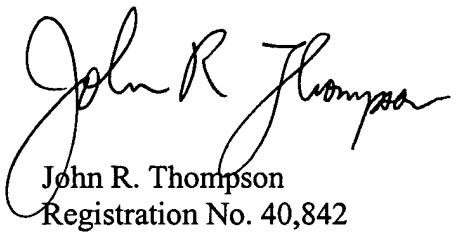
a. ☐ each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

b. ☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.

3. ☐ Applicant(s) set forth below concise explanations of the relevance of each document not in the English language and/or selected document(s) in the English language.

DATED this 31 day of October, 2003.

Respectfully submitted,



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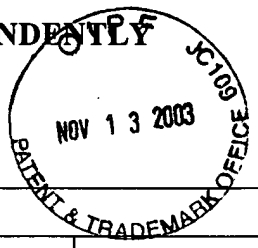
Sheet 1 of 7

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/2 US	APPLICATION NO. 10/613,169
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET**		FILING DATE- July 3, 2003	



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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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	20							
	21							
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	62	Ieong et al., "High Performance Double-Gate Device Technology Challenges and Opportunities," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY, USA, pgs. 492-495.
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EXAMINER	DATE CONSIDERED

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